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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/069,088	04/29/98	LIANG S	06502.0129-0

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EXAMINER	
NGUYEN, V	
ART UNIT	**PAPER NUMBER**
2755	5

DATE MAILED: 07/05/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/069,088	SHENG LIANG
Examiner	**Group Art Unit**
Van Nguyen	2755

☒ Responsive to communication(s) filed on *Apr 29, 1998*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-25* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-25* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *4*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

DETAILED ACTION

1. Claims 1-25 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by **Richardson** (**U.S.PAT.NO. 5,974,536**; hereinafter **Richardson**).

As to claims 1, 9, 17, and 25, Richardson teaches (col.4, lines 30-67) time profiling multiple threads of execution (profiling virtual memory access by one or more threads), a program (program thread), interrupting (interrupts) execution of all of the threads (program thread), determining (having) whether register data (placement data) corresponding to a selected thread

(the respective thread) has changed; and providing an indication (assemble code identified) of the change for the selected thread.

As to claims 2, 10, and 18, Richardson teaches (col.4, lines 30-67; col.5, lines 30-50) accessing stored data corresponding to the selected thread (virtual memory addresses are accessed by each thread); and comparing the stored data with register information stored following a previous interrupt (analyzes virtual memory accesses by one or more threads).

As to claims 3, 11, and 19, Richardson teaches (col.6, lines 5-67) computing a value corresponding to the stored data; and determining a relationship between the computed value and the previously stored register information.

As to claims 4, 12, and 20, Richardson teaches (col.5, lines 35-67) updating a memory segment (analyzes which regions of virtual memory are accessed by each program thread) to reflect that the selected thread is running when it is determined that the computed value and the previously stored register information do not match.

As to claims 5, 13, and 21, Richardson teaches (col.4, lines 30-67 and col.6, lines 1-67) a selected thread (a thread), a multi-threaded program (program thread), suspending (interrupts) execution of the multi-threaded program (program thread), retrieving register data (register) corresponding to the selected thread, computing a value (determines a valid load) based on the register data, comparing (the histogram generator walks...stored instruction is reached) the computed value with register information stored following a previous suspension of the multi-threaded program, and regarding (histogram data for each thread...upon particular

performance needs) the selected thread as running if the computed value is different from the previously stored register information.

As to claims 6, 14, and 22, Richardson teaches (col.6, lines 45-67) updating (a histogram is then incremented) the previous register information based on the computed value.

As to claims 7, 15, and 23, Richardson teaches (col.4, lines 35-67) providing an indication (assembly code identified by the returned program counter) corresponding to a portion of the program containing the selected thread.

As to claims 8, 16, and 24, Richardson teaches (col.4, lines 35-67 and col.6, lines 1-67) time profiling multiple threads (profiling virtual memory access by one or more threads), a program (program thread), suspending (interrupts) execution of the program; determining (operating system sets a PC to reference) whether stored information corresponding to processor registers for each thread (the thread) indicates that the thread is running (the thread being run), and recording (recorded in a histogram) time-profiling information for each running thread.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Doing et al. (U.S.PAT. NO.6,018,759) teaches "Thread Switch Tuning Tool For Optimal Performance In A Computer Processor."

b) Agrawal et al. (U.S.PAT. NO.5,768,500) teaches "Interrupt-Based Hardware Support For Profiling Memory System Performance."

c) Jackson (U.S.PAT. NO.5,297,274) teaches "Performance Analysis Of Program IN Multithread OS By Creating Concurrently Running Thread Generating Breakpoint Interrupts To Active Tracing Monitor."

d) Eickemeyer et al. (U.S.PAT. NO.6,061,710) teaches "Multithreaded Processor Incorporating A Thread Latch Register For Interrupt Service New Pending Threads."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Van Nguyen whose telephone number is (703) 306-5971. The examiner can normally be reached on Monday-Friday from 8:00AM to 5:00PM.

ALVIN E. OBERLEY
SUPERVISORY PATENT EXAMINER
GROUP 2700